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Your reference IP/P7207

Patent application number *(The Patent Office will fill in this part)* 0326993.3

20 NOV 2003

Full name, address and postcode of the or of each applicant *(underline all surnames)*

QINETIQ LIMITED

Registered Office 85 Buckingham Gate
London SW1E 6PD
United Kingdom

atents ADP number *(if you know it)*

8307431001

If the applicant is a corporate body, give the country/state of its incorporation

GB

Title of the invention

STRAINED SEMICONDUCTOR DEVICES

Name of your agent *(if you have one)*

Philip Davies et al

Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

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Patents ADP number *(if you know it)*

8183873001

| | Country | Priority application number *(if you know it)* | Date of filing *(day / month / year)* |
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Signature P Davies — Date 18 Nov 2003

12. Name and daytime telephone number of person to contact in the United Kingdom — Linda Bruckshaw 01252 392722

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DUPLICATE

# Strained Semiconductor Devices

The present invention relates to semiconductor devices in which a narrow bandgap semiconducting region is subject to strain.

Narrow bandgap semiconductors such as indium antimonide InSb have useful properties such as very low electron effective mass, very high electron mobility and high saturation velocity. These are potentially of great interest for ultra high-speed transistor applications. InSb in particular is a promising material for fast very low power dissipation transistors, because its electron mobility $\mu_e$ at low electric fields is nine times higher that than of GaAs, and its saturation velocity $v_{sat}$ is more than five times higher, despite GaAs having better properties than silicon in these respects. InSb is also predicted to have a large ballistic mean free path of over 0.5 microns. This suggests that InSb would be very suitable for high-speed low voltage operation, and the consequent low power consumption would make it ideal for portable and high device-density applications.

The application of strain to a semiconductor is an established way of altering its characteristics. While it has chiefly been applied to electro-optic devices such as lasers and photodetectors, US 5,382,814 discloses a MISFET which includes an $Al_xIn_{1-x}Sb$ layer which contains 15% Al. This layer is expansively strained because the addition of the Al atoms into the lattice reduces the lattice constant relative to the adjacent material. However, in this prior art $p^+p^+$(wide gap)$p^-n^+$ structure the $Al_xIn_{1-x}Sb$ wide gap layer is intended to act as a barrier in the conduction band to prevent electrons from moving from the $p^+$ contact region into the $p^-$ active region. It does not act as a layer in and along which carrier transport occurs, and the presence of strain therein is not fundamental to operation of the device.

It is now appreciated that it is possible to construct transistors with a compressively strained region or layer where the presence of the strain usefully affects the transistor properties.

Accordingly the present invention provides a transistor including at least one narrow bandgap region or layer that is doped p-type or contains an excess of holes and is subject to compressive mechanical strain.

Preferably the narrow bandgap is no more than 1.0 eV, preferably no more than 0.75 eV, and most preferably no more than 0.5 eV. In materials with such narrow bandgaps the strain effect on the bands is most likely to be large enough to be useful.

The compressive mechanical strain may be imposed upon the narrow bandgap region by being adjacent at least one further layer or region having a different lattice constant. Preferably there is at least one further layer or region on each of two opposed sides of the narrow bandgap layer or region.

In devices according to the invention the majority carriers in the strained region will be holes. Commonly, the strained region or layer will be one permitting carrier transport in use and often will be the one in which the main carrier transport occurs, e.g. in and along such a layer.

The invention may be applied inter alia to FETs, for example p-channel quantum well effect FETs, and also to bipolar transistors, e.g. n-p-n transistors.

Our International Patent Application No. PCT/GB03/01148 discloses and claims a quantum well field effect transistor wherein the quantum well is provided by a primary conduction channel and at least one secondary conduction channel immediately adjacent and in contact with the primary channel, the secondary channel having an effective bandgap greater than the effective bandgap Eg (effective) of the primary channel, wherein the modulus of the difference between the effective impact ionisation threshold IIT (effective) and the effective conduction band offset $\Delta E_C$ (effective) between the primary and secondary channels being no more than 0.5 Eg (effective). It also discloses and claims a quantum well field effect transistor wherein the quantum well is provided by a primary conduction channel and at least one secondary conduction channel immediately adjacent and in contact with the primary channel, the secondary channel having an effective bandgap greater than the effective bandgap Eg (effective) of the primary channel, wherein the modulus of the difference

between the effective impact ionisation threshold IIT (effective) and the effective conduction band offset $\Delta E_C$ (effective) between the primary and secondary channels being no more than 0.4 eV.

Our earlier UK Patent Application Serial No. 2 362 506 discloses and claims an extracting transistor characterised in that (a) it is a field effect transistor incorporating a conducting region consisting at least partly of a quantum well; (b) the quantum well is in an at least partly intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and (c) it includes at least one junction which is biasable to reduce the intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

Our International Patent Application No. PCT/GB02/05904 discloses and claims a bipolar transistor with a vertical geometry having a base region provided with a base contact, emitter and collector regions arranged to extract minority carriers from the base region, and a structure for counteracting entry of minority carriers into the base region via the base contact, wherein the base region has a bandgap of greater than 0.5 eV and a doping level greater than $10^{17}$ $cm^{-3}$. In a structure of this type the base can be compressively strained to allow light hole transport as is necessary in an efficient n-p-n device.

In addition, our International Patent Application No. PCT/GB01/02284 discloses and claims a bipolar transistor having emitter and collector regions arranged to extract minority carriers from the base region, a structure for counteracting entry of minority carriers into the base region via the base contact, the base region having a band gap less than 0.5 eV and wherein the base region has a doping level greater than $10^{17}$ $cm^{-3}$.

While the present invention is not limited to these prior art constructions, such quantum well FETs and bipolar transistors may be based inter alia on InSb. In such a case the presence of an $Al_xIn_{1-x}Sb$ layer or layers having a significantly lower lattice constant will introduce a strongly compressive strain into the quantum well or base region respectively. The strain effect in the InSb material is very strong and in

principle allows the energies of the light and heavy holes to be split by an amount much greater than kT. As the mobility of the light holes in InSb (in a lower energy band than the heavy holes) is almost as great as that of the electrons (and much greater than the mobility of the heavy holes which normally predominate transport in unstrained InSb), this gives rise to the possibility of making high performance hole-based devices. When the latter devices are used in conjunction with the corresponding but more conventional electron-based ones, this permits the design of very high-speed low power complementary logic circuits having good circuit performance and low quiescent power consumption.

The strain effect is strong in InSb and accordingly a preferred material for the compressively strained narrow band-gap region is InSb. However, it is possible to use other materials such as InAs in a similar manner in transistors according to the invention.

Further features and advantage of the invention will become clear upon a perusal of the appended claims, to which the reader is directed, and upon consideration of the following more detailed description of embodiments of the invention, made with reference to the accompanying drawings, in which:

Figure 1 shows in diagrammatic cross-section a quantum well FET according to the invention;

Figure 2 illustrates pictorially the effect of compressive strain on a quantum well layer of the type illustrated in the transistor of Figure 1;

Figure 3 shows calculated dispersions for a quantum well transistor of the type illustrated in Figure 1; and

Figure 4 shows in diagrammatic cross-section a bipolar transistor according to the invention.

In Figure 1 an optional highly n-type doped back contact layer 2 for carrier extraction lies directly upon an insulating substrate 1, for example of GaAs. A layer 5 of InSb which is modulation doped or directly doped with p-type dopants forms a quantum

well between layers 4 and 6 of $In_{1-x}Al_xSb$. If used, modulation doping is provided by sheets of dopant between layers 6 and 7, or between layers 3 and 4, or between both. A further layer 3 of $In_{1-x}Al_xSb$ lies between layer 4 and the back contact 2, and another layer 7 of $In_{1-x}Al_xSb$ overlies the layer 6. Connections to each end of the p-type conduction channel are provided p-type contacts 8, 9 and overlying metallic contacts 10, 11 respectively, and a Schottky gate (or an oxide based gate) 12 is provided to control channel conduction.

The value of x in the layers 4 and 6 is high enough to induce sufficient strain in the layer 5 that the light and heavy holes are separated by an amount much greater than kT.

Typical values of layer thickness and x are as follows:

| | | |
|---|---|---|
| Layer 2: | 0.5-3 $\mu$m thick; | x = 0.15-0.30 |
| Layer 3: | 0.5-0.75 $\mu$m thick; | x = 0.15-0.30 |
| Layer 4: | 3-10 nm thick; | x = 0.15-0.30 |
| Layer 5: | 5-20 nm thick; | |
| Layer 6: | 3-10 nm thick; | x = 0.15-0.30 |
| Layer 7: | 10-20 nm thick; | x = 0.15-0.30 |

Figure 2 illustrates pictorially the effect of compressive strain on band structure, for example in a quantum well transistor of the general construction of Figure 1, and the crossing of the heavy and light hole bands in-plane is to be noted, whereas the two bands separate orthogonal to the plane.

Figure 3 shows the calculated in-plane sub-band dispersions for a quantum well transistor of the general construction of Figure 1, with an InSb quantum well between barriers of $In_{0.81}Al_{0.19}Sb$ in cases where the well is 5nm thick (Figures 2(a) and 2(b)), and 10 nm thick (Figures 2(c) and 2(d)). The plots provide good evidence for the existence of "heavy" and "light" holes. Initial calculations suggest that a sheet hole density in the $10^{11}$ to $10^{12}$ $cm^{-1}$ range is achievable with the holes having a mobility comparable to the electron mobility, giving the potential for a good matching of device characteristics in complementary device circuitry.

Figure 4 shows an n-p-n bipolar transistor in which the base region 19 is of p-type doped InSb. The base also comprises the base contact metal 13 upon a $p^+$ layer 14. A further $p^+$ layer 15 lies between and in contact with the region 19 and the layer 14. The emitter comprises the emitter contact metal 16 upon an $n^+$ layer 17. A further $n^+$ layer 18 lies between and in contact with the layer 17 and the base region 19. The collector comprises an $n^+$ layer 22 between and in contact with a semi-insulating substrate 23 and the n collector layer 20. There is an ohmic contact metal layer 21 upon layer 22, and the layer 20 lies between and in contact with the layer 22 and the base region 19. Each of layers 15, 18, 20 and 22 are of wider bandgap (and smaller lattice constant) $Al_xIn_{1-x}Sb$, the presence of which imparts a compressive strain to the narrower bandgap base layer 19. The construction should allow the base layer 20 to be strained, thereby affording light hole transport and permitting faster device speed with lower base access resistance for improved power gain.

Typical values of layer thickness and x are as follows:

| | | |
|---|---|---|
| Layer 14: | 5-20 nm thick | |
| Layer 15: | 5-20 nm thick | x = 0.15-0.30 |
| Layer 17: | 5-20 nm thick | |
| Layer 18: | 5-20 nm thick | x = 0.15-0.30 |
| Layer 19: | 5-20 nm thick | |
| Layer 20: | 0.3-2 $\mu$m thick | x = 0.15-0.30 |
| Layer 22: | 0.5-5 $\mu$m thick | x = 0.15-0.30 |

CLAIMS

1. A transistor including at least one narrow bandgap region or layer that is doped p-type or contains an excess of holes and is subject to compressive mechanical strain.

2. A transistor according to claim 1 wherein said narrow bandgap region or layer is arranged for majority carrier transport.

3. A transistor according to claim 1 or claim 2 wherein said narrow bandgap region or layer is in contact with at least one further region or layer having a different lattice constant whereby said narrow bandgap region or layer is subject to said compressive mechanical strain.

4. A transistor according to any preceding claim wherein there are at least two said further layers, one on each side of said narrow bandgap region or layer.

5. A transistor according to any preceding claim wherein said narrow bandgap region or layer comprises InSb or InAs.

6. A transistor according to any preceding claim wherein the transistor is a quantum-well FET.

7. A transistor according to claim 6 wherein the quantum well is provided by a primary conduction channel and at least one secondary conduction channel immediately adjacent and in contact with the primary channel, the secondary channel having an effective bandgap greater than the effective bandgap Eg (effective) of the primary channel, wherein the modulus of the difference between the effective impact ionisation threshold IIT (effective) and the effective conduction band offset $\Delta E_C$ (effective) between the primary and secondary channels being no more than 0.5 Eg (effective).

8. A transistor according to claim 7 wherein the quantum well is provided by a primary conduction channel and at least one secondary conduction channel immediately adjacent and in contact with the primary channel, the secondary channel

having an effective bandgap greater than the effective bandgap Eg (effective) of the primary channel, wherein the modulus of the difference between the effective impact ionisation threshold IIT (effective) and the effective conduction band offset $\Delta E_C$ (effective) between the primary and secondary channels being no more than 0.4 eV.

9. A transistor according to claim 6 in the form of an extracting transistor characterised in that (a) it is a field effect transistor incorporating a conducting region consisting at least partly of a quantum well; (b) the quantum well is in an at least partly intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and (c) it includes at least one junction which is biasable to reduce the intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

10. A transistor according to any one of claims 1 to 5 wherein the transistor is an n-p-n bipolar transistor.

11. A transistor according to claim 10 with a vertical geometry having a base region provided with a base contact, emitter and collector regions arranged to extract minority carriers from the base region, and a structure for counteracting entry of minority carriers into the base region via the base contact, wherein the base region has a bandgap of greater than 0.5 eV and a doping level greater than $10^{17}$ $cm^{-3}$.

12. A transistor according to any preceding claim wherein the narrow bandgap is no more than 1.0 eV.

13. Complementary logic circuitry comprising a transistor according to any preceding claim.

14. An integrated circuit comprising a transistor according to any one of claims 1 to 12 or complementary logic circuitry according to claim 13.

15. A transistor substantially as hereinbefore described with reference to Figure 1 or Figure 4 of the accompanying drawings.

## ABSTRACT

In a transistor in which the majority carriers are holes, at least one narrow bandgap region or layer is doped p-type or contains an excess of holes and is subject to compressive mechanical strain, whereby hole mobility may be significantly increased. In a p-channel quantum well FET, the quantum well InSb well p-type layer 5 (modulation or directly doped) lies between $In_{1-x}Al_xSb$ layers 4, 6 where x is of a value sufficient to induce strain in layer 5 to an extent that light and heavy holes are separated by much more than kT. Transistors falling within the invention, including bipolar pnp devices, may be used with their more conventional electron majority carriers counterparts in complementary logic circuitry.

(Figure 1 should accompany the abstract)

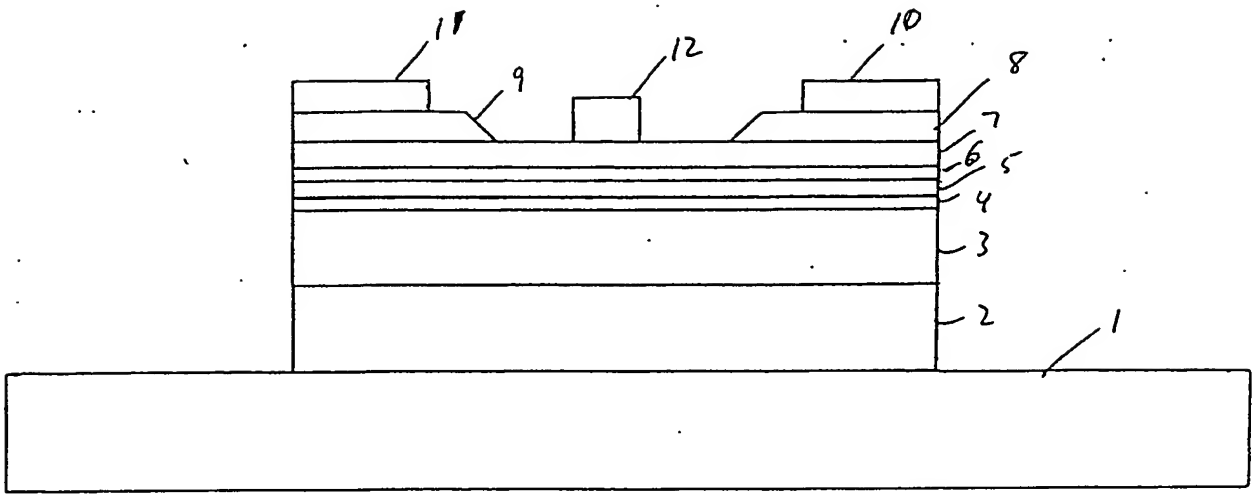



Figure 1

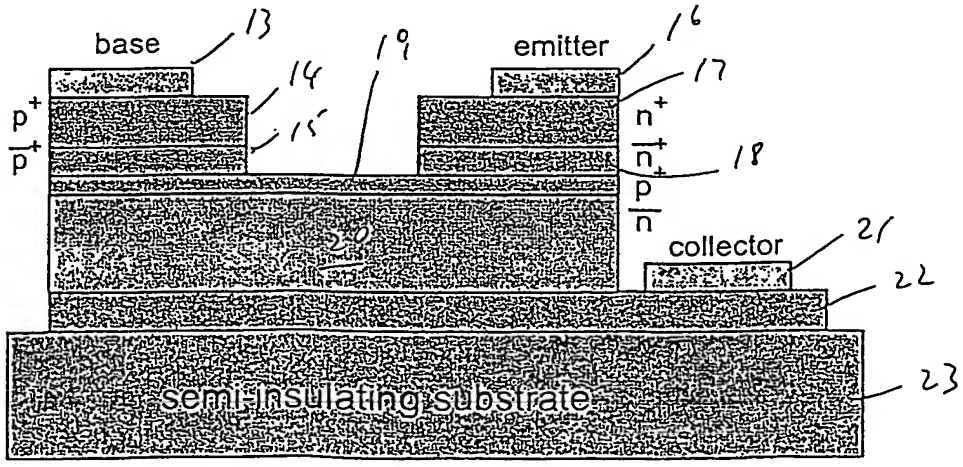
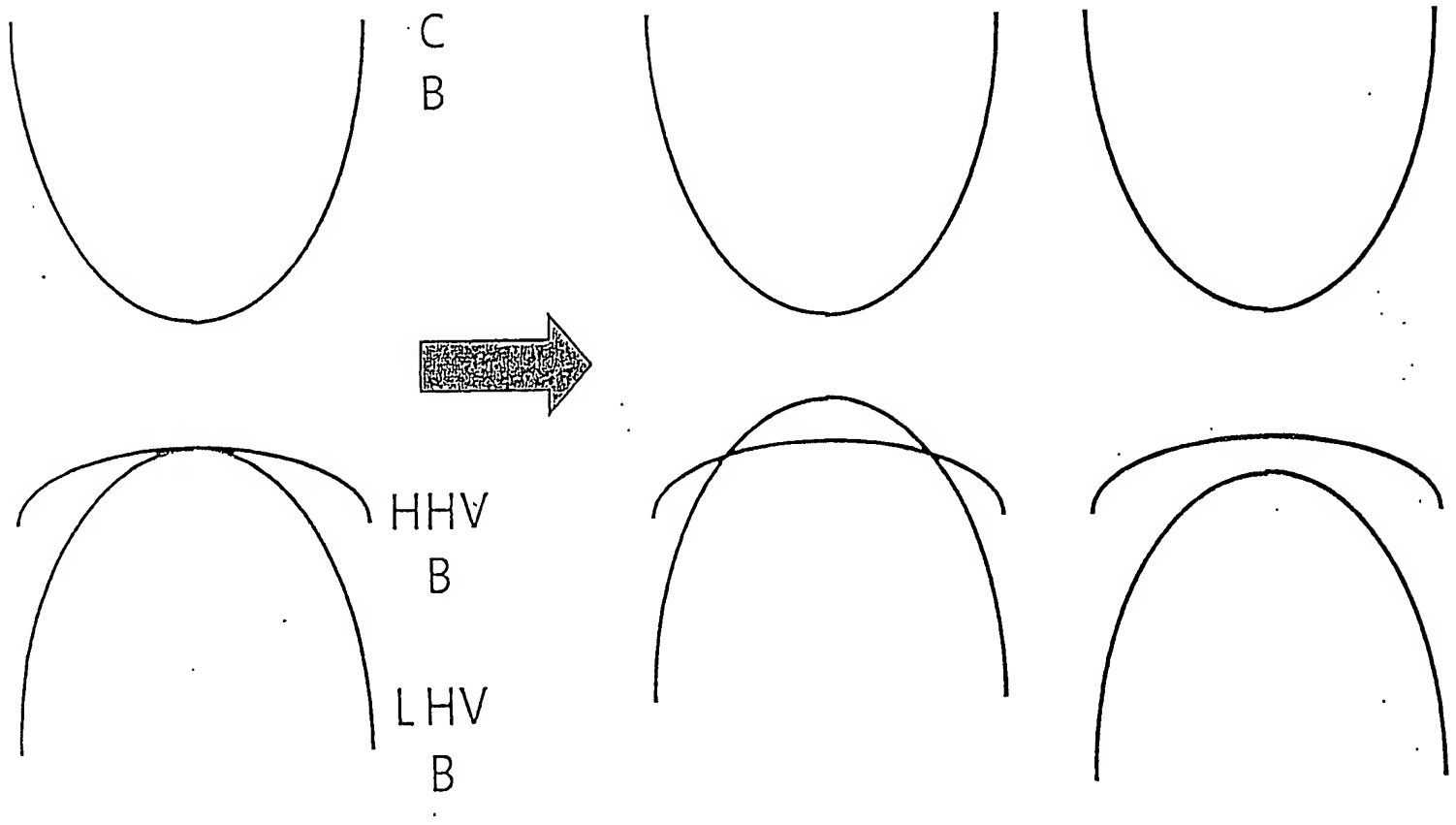



Figure 4

# Effect of Compressive Strain on Band Structure




- For example, InSb QW in AlInSb barrier

Figure 2

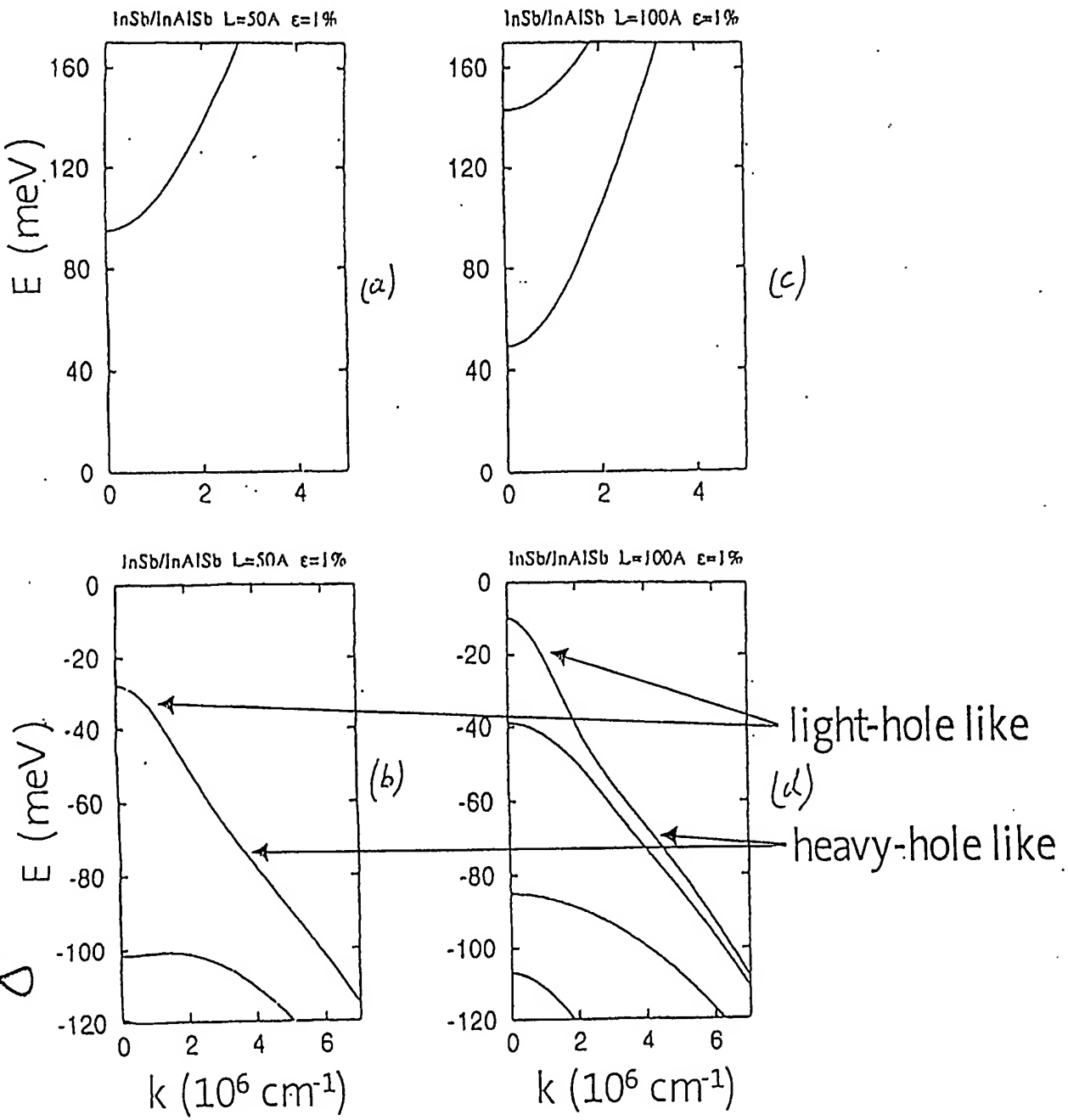

InSb/InAlSb L=50A ε=1%
InSb/InAlSb L=100A ε=1%
E (meV)
160
120
80
40
0
0
2
4
(a)
(c)
InSb/InAlSb L=50A ε=1%
InSb/InAlSb L=100A ε=1%
0
-20
-40
-60
-80
-100
-120
0
2
4
6
(b)
(d)
light-hole like
heavy-hole like
k (10⁶ cm⁻¹)
k (10⁶ cm⁻¹)

Figure 3

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